REMARKS

Claims 1-9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the applicants' admitted prior art (AAPA) of this application in view of Liu, et al. (U.S. Patent No. 6,248,641). In view of the amendments to claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

The applicants' invention is directed to a method of fabricating a non-volatile memory device. A tunnel insulating layer, a floating gate conductive layer and a first insulating layer are formed sequentially over a semiconductor substrate. The floating gate conductive layer serves as the floating gate in a transistor device formed as part of the memory device. A second insulating layer is formed over the structure after trenches are etched, and the second insulating layer is selectively removed to form element isolation regions composed of the trenches filled with the second insulating layer. The first insulating layer is then removed and the second insulating layer is selectively removed using chemical mechanical polishing (CMP). During this CMP process, the floating gate conductive layer is used as a stopping layer.

Hence, in accordance with the invention, the conductive layer that is to be used as the floating gate of a transistor is used as the stopping layer during the CMP process. As a result, additional steps of removing the conductive etch stopping layer and then reforming a floating gate conductive layer are eliminated. The claims are amended to clarify that the conductive layer, which is used as the stopping layer for the CMP process, is also used as the floating gate of a transistor in the memory device. It is believed that this clarifying claim language distinguishes the cited prior art.

The AAPA of the application does not show using a conductive floating gate layer as a stopping layer during a CMP process. Also, Liu, et al. fail to teach or suggest using a conductive layer that serves as a floating gate of a transistor as a stopping layer during the CMP process. Specifically, referring to Liu, et al. at Figure 2F and the description at column 3, lines 10-14, a

polysilicon layer 21 serves as an etch stopping layer during a CMP process. However, the polysilicon layer 21 is removed after the CMP process. As a result, the polysilicon layer 21 is not used as a floating gate in a transistor forming part of the Liu, et al. device, as set forth in the amended claims. In Liu, et al., if a transistor is to be formed after the CMP process, a new floating gate conductive layer would have to be added. Accordingly, Liu, et al. also fail to teach or suggest the invention set forth in the amended claims.

Since neither of the AAPA and the Liu, et al. references teaches or suggests the invention set forth in the amended claims, no combination of the references could result in teaching or suggesting the invention. Since neither of the cited references, taken alone or in combination, teaches or suggests the invention set forth in the amended claims, it is believed that the claims are allowable over the cited references. Therefore, reconsideration of the rejections of the claims under 35 U.S.C. § 103(a) based on the AAPA and Liu, et al. is respectfully requested.

Independent claim 1 is amended to incorporate the subject matter of dependent claim 2, and claim 2 has been cancelled. Since claim 2 was in the application as filed, it has been searched and considered, therefore, it is believed that entry of this Amendment would not require additional consideration and/or search. It is also believed that entry of the amendment would place the application in condition for allowance.

Attached hereto is a marked-up version of the changes made to the claims and specification by the current Amendment. The attached page is captioned "Version with Markings to Show Changes Made".

In view of the amendments to the claims and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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Steven M. Mills
Registration Number 36,610
Attorney for Applicants

Mills & Onello LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
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Version with Markings to Show Changes Made

In the claims:

Claim 2 has been cancelled.

Claim1, 3, 7 and 9 have been amended as follows:

1. (Twice Amended) A method of fabricating a non-volatile memory device having a tunnel insulating layer, comprising:

sequentially depositing said tunnel insulating layer, a floating gate conductive layer, and a first insulating layer over a semiconductor substrate, said tunnel insulating layer including at least two portions of different thicknesses, and said conductive layer serving as a floating gate in a transistor device formed as part of a memory cell in the memory device;

selectively etching the resultant structure to a given depth to form trenches;

depositing a second insulating layer over said structure including said trenches;

selectively removing said second insulating layer so as to form element isolation regions composed of the trenches filled with said second insulating layer;

removing said first insulating layer; and

selectively removing said second insulating layer using a chemical mechanical polishing (CMP) process until a surface of the floating gate conductive layer is substantially even with a surface of the second insulating layer, the floating gate conductive layer being used as a stopping layer for the CMP process.

3. (Amended) A method as defined in Claim 1, wherein said floating gate conductive layer has a thickness of 50 to 1000Å.

7. (Amended) A method as defined in Claim 6, wherein the step of selectively removing said flattened first insulating layer is performed until said floating gate conductive layer is exposed.

9. (Amended) A method as defined in Claim 1, wherein the step of selectively removing said second insulating layer by the CMP process employs a slurry with selectivity between said second insulating layer and the floating gate conductive layer equal to or greater than 1.